DPP
DAILY PRACTICE PROBLEMS

Class : XIIth
Date :

Solutions

Subject : PHYSICS
DPP No. : 9

Topic :- SEMICONDUCTOR ELECTRONICS: MATERIALS,DEVIES AND SIMPLE CIRCUITS

1 **(c)**

The emission current $i = AT^2Se^{-\phi/kT}$

For the two surfaces $A_1 = A_2, S_1 = S_2, T_1 = 800\ K,$

$T_2 = 1600\ K, \phi_1/T_1 = \phi_2/T_2$

Therefore, $\frac{i_2}{i_1} = \left(\frac{T_2}{T_1}\right)^2 = (2)^2 = 4 \Rightarrow i_2 = 4i_1 = 4\ mA$

2 **(b)**

Depletion layer is more in less doped side

3 **(d)**

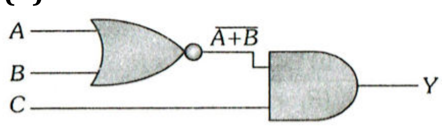
$\sigma = ne(\mu_e + \mu_h) = 2 \times 10^{19} \times 1.6 \times 10^{-19}(0.36 + 0.14)$

$= 1.6\ (\Omega - m)^{-1}$

$$R = \rho \frac{l}{A} = \frac{l}{\sigma A} = \frac{0.5 \times 10^{-3}}{1.6 \times 10^{-4}} = \frac{25}{8}\Omega$$

$$\therefore i = \frac{V}{R} = \frac{2}{25/8} = \frac{16}{25}A = 0.64\ A$$

4 **(d)**



The output Y is

$Y = \overline{(A + B)} \cdot C$

The truth table of the given circuit is as shown in the table

A	B	C	$\overline{A + B}$	$Y = \overline{(A + B)}.C$
0	0	0	1	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

5 **(b)**

In circuit the upper diode junction is forward biased and the lower diode junction is reverse biased. Thus there will be no conduction across lower diode junction. Now the total resistance of circuit $= 100 + 150 + 50 = 300\Omega$

Current in $100\Omega = \frac{6}{300} = 0.02$ A.

6 **(d)**

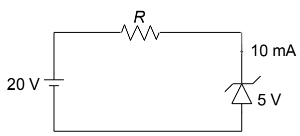
Among the given materials copper is the best conductor of electricity

7 **(d)**

Voltage available across load resistance

$R = 20 - 5 = 15$ V

Resistance of load,



$$R = \frac{15}{10 \times 10^{-3}} = 1.5 \times 10^3$$

$= 1.5$ kΩ

8 **(c)**

When a light (wavelength sufficient to break the covalent bond) falls on the junction, new hole electron pairs are created. No. of produced electron hole pairs depend upon no. of photons. So photo $e.m.f$. or current is proportional to intensity of light

9 **(a)**

Let I_e be the emitter current.

$\therefore \quad \frac{90}{100} \times I_e = I_c$

$\Rightarrow \quad I_e = \frac{100\, I_c}{90} = \frac{10}{9} I_c$

$$\therefore \alpha = \frac{I_c}{I_e} = \frac{9}{10} = 0.9$$

And

$$\beta = \frac{I_c}{I_e} = \frac{I_c}{I_e - I_c} = \frac{1}{\frac{I_e}{I_c} - 1} = \frac{1}{\frac{10}{9} - 1} = \frac{9}{1} = 9$$

10 **(d)**

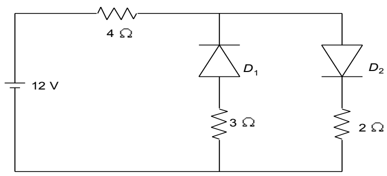
5 $volt$ is low signal (0) and 10 $volt$ is high signal (1) and taking 5 μ-s as 1 unit, in a negative logic, low signal (0) gives high output (1) and high signal (1) gives low output (0). The output is therefore 1010010111

11 **(b)**

It is used to convert ac into dc (rectifier)

12 **(b)**

In the given circuit diode D_1 is reverse biased while D_2 is forward biased, so the ircuit can be redrawn as



[∵ For ideal diodes, reverse biased means open and forward biased means short]

Apply KVL to get current flowing through the circuit.

$-\ 12 + 4i + 2i = 0$

$\Rightarrow\ = \dfrac{12}{6} = 2\,A$

14 **(c)**

Here $p - n$ junction is forward biased. If $p - n$ junction ideal, its resistance is zero. The effective resistance across A and B

$= \dfrac{10 \times 10}{10 + 10} = 5\text{k}\Omega.$

Current in the circuit $I = \frac{V}{R} = \frac{30}{15 \times 10^3} = \frac{2}{10^3}$ A

Current in arm $AB = I = \frac{2}{10^3}$

Potential difference across A and $B = \frac{2}{10^3} \times 5 \times 10^3 = 10$ V.

15 **(b)**

Due to forward bias at the emitter-base junction, the majority charge carrier electrons of emitter get repelled from the negative terminal and move towards base. Some of these electrons combine with the majority charge carrier holes present in the base and most of the electrons reach the collector, crossing the collector-base junction. This implies that collector current is always less than the emitter current due to the reason (b).

16 **(a)**

In P-type semi conductor, holes are majority charge carriers

17 **(d)**

n-p-n transistor is formed by combining two n-types crystals between which a thin p-type crystal is there. Electrons are charge carriers within the *n-p-n* transistor whereas holes are charge carriers within the *p-n-p* transistor. Since, electrons move more easily than holes, hence *n-p-n* transistors are preferred compared to *p-n-p.*

18 **(d)**

At logic gate I, the Boolean expression is $\overline{B} \cdot C = Y'$

At logic gate II, the Boolean expression is $A + (\overline{B} \cdot C) = Y''$

At logic gate III, the Boolean expression is $\overline{A + (\overline{B} \cdot C)} = Y$

19 **(c)**

In circuit A, both $(p - n)$ junction diode act as forward biased. Hence, current flows in circuit A,

Total resistance R is given by

$\dfrac{1}{R} = \dfrac{1}{4} + \dfrac{1}{4} \Rightarrow \dfrac{1}{R} = \dfrac{2}{4} \Rightarrow R = 2\Omega$

According to Ohm's law

$V + I_A R \Rightarrow 8 = I_A \times 2 \Rightarrow I_A = 4\ A$

In circuit B, lower P-N junction diode is reverse biased. Hence, no current will flow but upper diode is forward biased, so current can flow through it

$V = I_B R \Rightarrow 8 = I_B \times 4 \Rightarrow I_B = 2\ A$

20 **(d)**

For tetragonal, cubic and orthorhombic system $\alpha = \beta = \gamma = 90°$

ANSWER-KEY										
Q.	1	2	3	4	5	6	7	8	9	10
A.	C	B	D	D	B	D	D	C	A	D
Q.	11	12	13	14	15	16	17	18	19	20
A.	B	B	D	C	B	A	D	D	C	D